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APPLICATION NO.	FI	LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,087	03/31/2004		Takahiro Ochiai	HITA.0535	5095
7590 03/23/2006				EXAMINER	
Stanley P. Fis	sher		SANEI, HANA ASMAT		
Reed Smith LI	.P				
Suite 1400				ART UNIT	PAPER NUMBER
3110 Fairview Park Drive				2879	
Falls Church, VA 22042-4503				DATE MAILED: 03/23/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

·			Y			
	Application No.	Applicant(s)				
	10/813,087	OCHIAI ET AL.				
Office Action Summary	Examiner	Art Unit				
·	Hana A. Sanei	2879				
The MAILING DATE of this communication app Period for Reply	pears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING D. - Extensions of time may be available under the provisions of 37 CFR 1.1 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period of Failure to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tin will apply and will expire SIX (6) MONTHS from , cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
1)⊠ Responsive to communication(s) filed on <u>31 M</u>	larch 2004.					
	action is non-final.					
,—	opplication is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under E						
• •						
Disposition of Claims						
4) Claim(s) <u>1-9</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdra	wn from consideration.					
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-9</u> is/are rejected.						
7) Claim(s) is/are objected to.	tti					
8) Claim(s) are subject to restriction and/o	r election requirement.	•				
Application Papers						
9)⊠ The specification is objected to by the Examine	er.					
10)⊠ The drawing(s) filed on 31 March 2004 is/are:	a)⊠ accepted or b)⊡ objected t	o by the Examiner.				
Applicant may not request that any objection to the						
Replacement drawing sheet(s) including the correc	tion is required if the drawing(s) is ob	jected to. See 37 CFR 1.121(d).				
11) ☐ The oath or declaration is objected to by the Ex	caminer. Note the attached Office	Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
12)⊠ Acknowledgment is made of a claim for foreign	priority under 35 U.S.C. § 119(a)-(d) or (f).				
a) ⊠ All b) □ Some * c) □ None of:	promy and a control of the control	, (-) - ()				
1. ☑ Certified copies of the priority document	s have been received.					
2. Certified copies of the priority document		ion No				
3. Copies of the certified copies of the prior						
application from the International Burea						
* See the attached detailed Office action for a list		ed.				
Attachment(s)	رسا . -	(DTO 440)				
Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948)	· 4) Interview Summary Paper No(s)/Mail D					
 Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) 	5) Notice of Informal F	Patent Application (PTO-152)				
Paper No(s)/Mail Date <u>3/31/04</u> .	6)					

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DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-5, 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Konya et al (JP 7-72508).

Regarding Claim 1, Konya teaches signal lines (address line terminal film, 31a; see at least Figs. 4-5) which are formed on an upper surface side of a substrate (1); wiring layers (31b) which are formed such that the wiring layers electrically connect one-side signal lines and another-side signal lines which define regions for forming terminal portions of the signal lines therebetween while obviating regions where the terminal portions of the signal lines are formed; and an insulation film (24) which has holes (24b) at regions forming the terminal portions (31a) and is formed so as to cover the signal lines and the wiring layer (Fig. 6)

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Regarding Claim 2, Konya teaches signal lines (address line terminal film, 31a; see at least Figs. 4-5) which are formed on an upper surface side of a substrate (1); an insulation film (24) which is formed such that the film covers the signal lines except for terminal portions of the signal lines; and conductive layers (31b) which extend in the extension direction of the signal lines such that the conductive layers traverse the terminal portions, wherein gaps (34) are formed between respective sides of the conductive layer parallel to the extension direction of the conductive layer, and the insulation film (24) and holes (24b) are formed in the signal lines at portions corresponding to the gaps along the extension direction of the signal lines.

Regarding Claim 4, Konya teaches gate signal lines (11, see at least Figs. 12-13), drain signal lines (16) and interlayer insulation films (23) which are formed between the respective signal lines (22) are formed on a display region, and a material of the insulation films (24, SiN, [0008]) is identical with a material of the interlayer insulation film (23, SiN, [0007]).

Regarding Claim 5, Konya teaches signal lines (22, see at least Fig. 13) which are formed on an upper surface side of the substrate (1); semiconductor layers (13) which are formed below the signal lines by way of a first insulation film (17) such that the semiconductor layers traverse the signal lines at terminal portions of the signal lines; a second insulation film (24) which is formed on the substrate such that the second insulation film also covers the signal lines and in which holes (24b, Fig. 6) are formed at regions thereof where the semiconductor layers are formed; and conductive layers (20) which have respective sides thereof in the extension direction of the signal lines

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arranged at both sides of the signal lines and are connected with respective semiconductor layers, wherein the resistance of the semiconductor layers is lowered [0016]. The applicant is claiming the product of a semiconductor including a method (i.e. a process) of lowering the resistance by introducing impurities there into using the signal lines as masks, consequently, Claim 5 is considered "product-by-process" claim. In spite of the fact that the product-by-process claim may recite only process limitations, it is the product and not the recited process that is covered by the claim. Further, patentability of a claim to a product does not rest merely on the difference in the method by which the product is made. Rather, it is the product itself that must be new and not obvious (see MPEP 2113). Accordingly, the method of lowering the resistance by introducing impurities there into using the signal lines as masks is not germane to the issue of patentability of the device/product itself and has not been given any patentable weight.

Regarding Claim 7, Konya teaches the display region includes thin film transistors (10) and a material of the semiconductor layers (13) is equal to a material of semiconductor layers (14) of the thin film transistors ([0004]).

Regarding Claim 8, Konya teaches the display region includes thin film transistors (10) and a material of the first insulation film (17, [0004]) is equal to a material of gate insulation films (12, [0004]) of the thin film transistors.

Regarding Claim 9, Konya teaches that the gate signal lines (11), drain signal lines (16) and interlayer insulation films (23) which are formed between the respective

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signal lines (22) are formed on a display region and a material of the second insulation film (24, [0008]) is identical with a material of the interlayer insulation films (23, [0007]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Konya et al (JP 7-72508) in view of Ono et al (US 6356331 B1) in further view of Ono et al (US 2002/0047970 A1) hereinafter referred to as '970.

Regarding Claims 3, 6, Konya teaches the invention set forth above (see rejection in Claim(s) 2 & 5 above) and further teaches gate signal lines (11) and drain signal lines (16). Konya lacks the material of the signal lines being equal to a material of the gate signal lines. In the same field of endeavor, Ono teaches the material of the signal lines (CL, Col. 5, lines 22-25) being equal to a material of the gate signal lines (GL) in order to achieve the advantage of preventing an increase in the number of manufacturing steps (Col. 5, lines 25-27). Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the materials, as disclosed by Ono, in the device of Konya in order to achieve the advantage of preventing an increase in the number of manufacturing steps.

semiconductor layer AS stated supra.

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Konya-Ono lacks the material of the conductive layer being equal to the material of the drain signal lines. In the same field of endeavor, '970 teaches the conductive layer (SD1; [0075]) being equal to the material of the drain signal lines (DL) in order to ensure the improvement in reliability of connection with the semiconductor layer AS stated supra ([0075]). Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the materials, as disclosed by Ono, in the device of Konya in order to ensure the improvement in reliability of connection with the

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hana A. Sanei whose telephone number is (571) 272-8654. The examiner can normally be reached on Monday- Friday, 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). 3/20/06 Roy 3/20/06 Roy 6:xhor 287

Examiner Hana A. Sanei